Three P-Silicon Layers in Reliable Lateral Double Diffused Metal Oxide Semiconductor Transistor

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Abstract— **Inserting three p-layers in the drift region and buried oxide of the Lateral Double Diffused MOSFET (LDMOS) is the main goal of this paper. One of these layers is considered in the drift region and two others are in the buried oxide. Moreover, these layers have different lengths. The new structure helps to have high breakdown voltage and low on-resistance that improves Figure Of Merit (FOM) in this power transistor. Also, replacing p-silicon layer instead of silicon dioxide under the drift region reduces lattice temperature and helps to have a reliable device. The electrical parameters of the novel structure are compared with the conventional one using ATLAS simulator.**

Keywords- LDMOS, Breakdown voltage, Specific on-resistance, Temperature.

I. Introduction

Nowadays power transistors are attracted by electronic industries for the high voltage applications. The breakdown voltage and specific on resistance are two main parameters in power transistors especially in Lateral Double Diffused Metal Oxide Semiconductors (LDMOSs) [1-6]. Silicon On Insulator (SOI) technology are widely used in MOSFET transistors [7-10]. Using silicon-on-insulator technology [11] in power transistors improves vertical breakdown voltage but in high breakdown voltage the devices suffer high temperate [12]. The insulator acts as a barrier for heat transfer and in the active region, the temperature increases which change the electrical characteristics such as drain current, mobility, off current and so on [13].

In this paper, a new LDMOS structure is proposed that high breakdown voltage occurs in lower temperatures. The purpose is achieved using three silicon P-layers in the device. These layers have different lengths. The first layer is considered in the drift region and the others are located in the buried oxide. The P-layers have high doping density than the drift region. This condition causes low specific on resistance and reduced lattice temperature in the device. Also, the breakdown voltage increases due to the different P-layers in the device. The new structure which is named as Three P^+ Layers in LDMOS Transistor (TPL-LDMOS) is simulated using two dimensional ATLAS simulator [14] and compared with Conventional LDMOS (C-LDMOS) structure.

II. Device Structure

The schematic cross section of the proposed structure is shown in Fig. 1. As it is clear, three silicon P-layers are considered in the drift regions and buried oxide like steps. The channel and drift lengths are 5 µm and 18 µm, respectively. the device parameters are listed in Table 1.

Table 1. The proposed structure parameters

Parameter	*Value*
Channel Length	5 µm
Drift Length	18 µm
P^+ layer 1 Length	6 µm
P^+ layer 2 Length	12 µm
P^+ layer 3 Length	18 µm
Buried Oxide Thickness	0.4 µm
P^+ layer 1 Thickness	0.2 µm
P^+ layer 2 Thickness	0.2 µm
P^+ layer 3 Thickness	0.2 µm
Top Silicon Thickness	0.6 µm
Channel Doping Concentration	1×10^{17} cm^{-3}
Source/Drain Doping Concentration	1×10^{20} cm^{-3}
Drift Doping Concentration	1×10^{15} cm^{-3}
P^+ Layer Doping Concentration	1×10^{17} cm^{-3}

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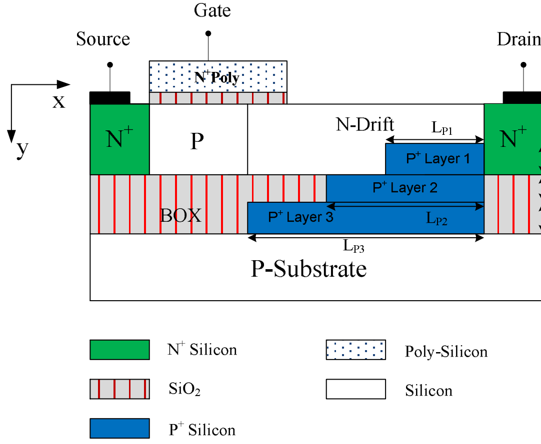

Figure 1. The schematic of TPL-LDMOS.

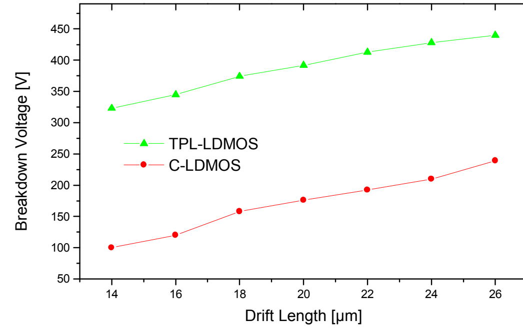

Figure 2. The breakdown voltage for the proposed and conventional structures.

III. RESULTS AND DISCUSSION

In this section, the proposed transistor is simulated using two dimensional ATLAS simulator and the results are compared with the conventional one. Considering P-layers in step form creates new peaks in the electrical field profile reducing the main peaks. So, the breakdown voltage increases. Fig. 2 shows the breakdown voltage versus drift length for both the proposed structure and the conventional one. The figure shows that the breakdown voltage increasing by increasing the drift length. However, the figure proves that the proposed structure has higher breakdown voltage.

As it was mentioned, the main peaks of the electric field are reduced in the proposed structure. So, the electron temperature reduces. Fig. 3 shows the electron temperatures for the proposed structure and the conventional one where they reducing by decreasing the drift length. It is clear that this temperature is significantly reduced in TPL-LDMOS and the reliability increases.

Silicon has higher thermal conductivity than SiO_2. In the proposed structure, silicon P-layers are considered instead of part of the buried oxide. So, the lattice temperature can be reduced. The lattice temperature along drift region is plotted in Fig. 4 for the proposed structure and the conventional one. The figure shows that TPL-LDMOS has smaller lattice temperature achieving more reliable device.

Drain current of the proposed structure and conventional one are compared in Fig. 5. Inserting three P^+ layers in the LDMOS device reduces on-resistance as it is clear in this figure. Also, silicon layer has higher thermal conductivity than buried oxide. So, in the TPL-LDMOS structure self-heating effect is controlled significantly. Higher drain current without negative slope in the saturation regime of the proposed structure is important which is the superiority of the proposed structure compared to the conventional one.

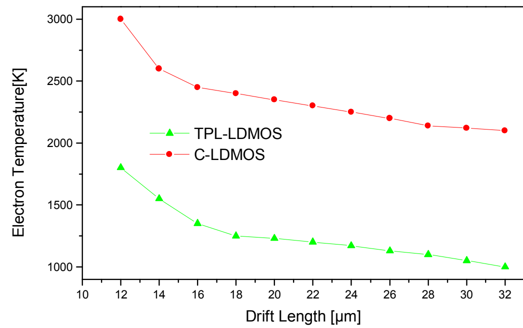

Figure 3. Electron temperature for for the proposed and conventional structures.

By reducing on-resistance and increasing the breakdown voltage, Figure Of Merit is improved. Moreover, more reliable device is achieved which can be used in power applications.

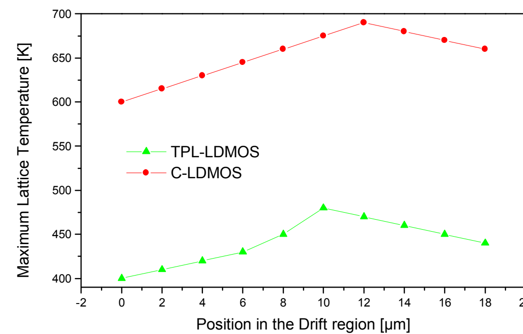

Figure 4. Maximum Lattice temperature for the proposed and conventional structures.

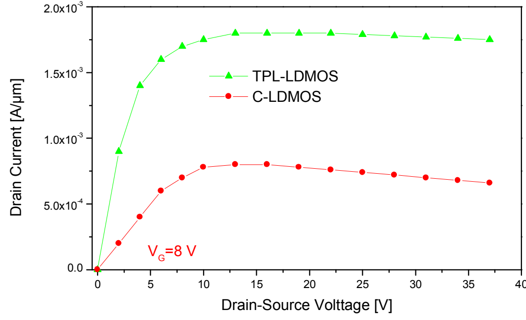

Figure 5. The drain current for the proposed and conventional structures

The on-resistance is an important parameter in transistors. Reducing on-resistance can be a goal for achieving better drain current. This parameter can be reduced by increasing the doping density. Considering silicon P-layer with higher doping density in the drift region reduces the on-resistance. Fig. 6 shows the specific on-resistance versus drift length for TPL-LDMOS and C-LDMOS. It is clear that the proposed structure has smaller on-resistance.

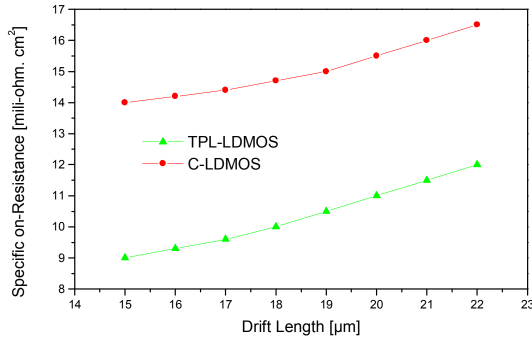

Figure 6. Specific on-resistance for the proposed and conventional structures.

The doping density of the three P^+ layers is essential to have the optimum behavior of the proposed structure. Higher doping density reduces on-resistance but reduces breakdown voltage, significantly. In Fig. 7 the variation of the breakdown voltage with doping density of three P^+ layers in two different drift lengths is shown. As it is clear the breakdown voltage has higher value in 1×10^{17} cm^{-3}. In this doping density the on-resistance has an acceptable value. So, this value is chosen for doping density of the three P+ layers.

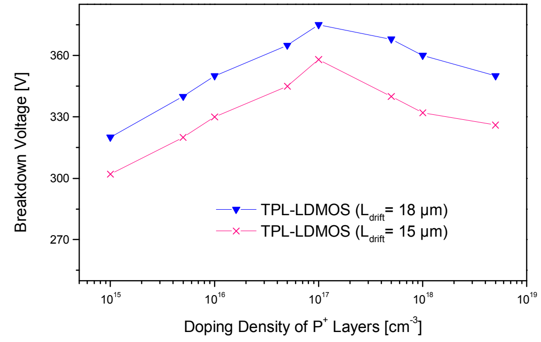

Figure 7. The variation of the breakdown voltage versus doping density of P^+ layers.

IV. CONCLUSION

A new SOI-LDMOSFET has been proposed in this paper to obtain more reliable device than the conventional one. In the new structure three silicon layers are inserted in drift region and buried oxide like the steps that improve the device parameters. Considering these steps causes more uniform electric field and consequently the breakdown voltage. Also, the electron temperature decreases. Moreover, because of more conductivity of silicon than oxide and considering this layer in the buried oxide reduces the lattice temperature. So, more reliable than the conventional one is obtain which simulating with two dimensional ATLAS simulator proves it.

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